8.5 Schematic for Three Stage Pipeline Design
Program Memory “Cache”
Immediate Operand Unit

Buf32

 Buf32

 INST0 INST1 INST2 INST3 INST4 INST5 INST6 INST7 INST8 INST9 INST10 INST11 INST12 INST13 INST14 INST15

Inst0 Inst1 Inst2 Inst3 Inst4 Inst5 Inst6 Inst7 Inst8 Inst9 Inst10 Inst11 Inst12 Inst13 Inst14 Inst15

Buf32

Buf32
3-Way 32-Bit Multiplexer
Register File

Schematic for Three Stage Pipeline Design
ALU and Equality Detector

Schematic for Three Stage Pipeline Design

Typical slice implemented using a PLA
ALU Slice implemented using Gates

Control Signal Conversion for use with Gate ALU Slice.
Barrel Shifter

Schematic for Three Stage Pipeline Design
Program Counter Parts

Branch Adder

Adder

Increment by 4

(Primitive type = adder)
Program Counter Parts, continued

4x32 Bus Multiplexer

32 Bit Register with Enable and Clear (see IR)
Data Memory

This page emulates a 4096 Word or 16384 Byte memory. Since it consumes two bytes of memory on the host machine and files for every byte it emulates, keep it small to be manageable.

Data Memory "Cache"

This gate detects addresses in the range 0x10000000 to 0x10003FFF so set your stack pointer to 0x10004000 and your global pointer to 0x10000000.
8.6 Five Stage Pipeline Design
Control Block for Five-Stage Pipeline

Decide and Operand Fetch Phase

Execute Phase

Memory Phase

Five Stage Pipeline Design